

USB4™ PCIe Tunneling Compliance Test Specification

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Revision History:

Revision	Issue Date	Comments
1.0	June 2020	First Release
1.1	January 2021	With clarifications and corrections
1.2	June 2021	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through October 15, 2020.
1.3	October 2021	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.4	March 2022	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.5	October 2022	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021.
1.6	December 2022	With corrections and clarifications. References the USB4 Specification, Version 1.0 with Errata and ECN through May 19, 2021 and includes additional ECN through October 2022.
2.0	November 2023	Revision that unites USB4 Version 1 and Version 2. Merge the changes from the USB4 Version 1 into USB4 Version 2 draft.
2.1	April 2026	Change AN_HUB_UFP1-PCIE_01 setup to AN_HUB_UFP2-PCIE_01. This makes the Hub UFP with downstream device consistent across CTSs. TD 11.006: Allow for link to train to L0 or L1. TD 11.020: Allow for link to train to L0 or L1.

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Introduction

The tests in this test specification verify that the Router in a USB4 Host, Hub, or Peripheral Device is compliant with Chapter 11 of the USB4™ Specification.

This specification applies to the following USB4 devices:

- A host with the USB4_PCIe_Tunneling_Supported parameter set to YES in the VIF
- A hub
- A peripheral the USB4_PCIe_Tunneling_Supported parameter set to YES in the VIF

Terminology

The following table describes the terms used in this document.

Analyzer	Test tool that captures and parses packets, transactions, ordered sets, etc.
Compliance Device	A KG USB4 Device that is capable of performing Transport Layer Packet loopback.
DFP	Downstream Facing Port.
Exerciser	The compliance test tool (hardware and software) that implements USB4 Port functionality and the behavior required for compliance testing.
IOP	Interop Testing. See USB4™ Interop Test Specification.
KG USB4 Device	“Known Good” USB4 Device. A USB4 Device that is known to be compliant with the USB4 Specification.
KG USB4 Host	“Known Good” USB4 Host. A USB4 Host that is known to be compliant with the USB4 Specification.
KG TBT3 Device	A Certified Thunderbolt 3 Device.
KG TBT3 Host	A Certified Thunderbolt 3 Host.
PUT	Port Under Test. The Port on a UUT that is being tested for compliance. Only Ports that support PCIe Tunneling are tested.
UFP	Upstream Facing Port.
USB4 CV	USB4 Command Verifier software. The software that runs compliance tests and analyzes the results.
USB4 Product	Refers to a USB4 host, USB4 hub, and/or USB4 device. Includes silicon, reference platforms, and end product.
UUT	The Router being tested for compliance.
VIF	Vendor Information File. File provided by UUT vendor that provides information about the characteristics and capabilities of the UUT.

Assertions

Compliance criteria are provided as a list of assertions that describe specific characteristics or behaviors that must be met. Each assertion provides a reference to the USB4 specification or other documents from which the assertion was derived. In addition, each assertion provides a reference to the specific test description(s) where the assertion is tested.

Each test assertion is formatted as follows:

Assertion #	Test #	Assertion Description
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Assertion#: Unique identifier for each spec requirement. The identifier is in the form USB4_SPEC_SECTION_NUMBER#X, where X is a unique integer for a requirement in that section.

Assertion Description: Specific requirement from the specification

Test #: A label for a specific test description in this specification that tests this requirement. Test # can have one of the following values:

- NT This item is not explicitly tested in a test description. Items can be labeled NT for several reasons – including items that are not testable, not important to test for interoperability, or are indirectly tested by other operations performed by the compliance test.
- X.X This item is covered by the test described in test description X.X in this specification.
- BCP This assertion is verified by the Background Check Procedure.

Test descriptions provide a high level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what the test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

Ver. 1 Assertions

The following Table presents the Chapter 11 assertions from the USB4 Ver. 1 Specification.

Assertion #	Test Name	Assertion Description
11 PCI Express Tunneling		
11#1	0	A USB4 host that tunnels PCIe traffic shall do one of the following: Incorporate an internal PCIe Switch; Connect to a Root Complex via Root Ports; Connect to a Root Complex via other means that meet the PCIe Specification.

11#2	NT	The Host Router in a USB4 host that supports PCIe Tunneling shall have one Downstream PCIe Adapter per Downstream Facing Port. Each Downstream PCIe Adapter shall interface to a downstream port of the internal PCIe Switch or Root Complex.
11#3	0	A USB4 hub shall support PCIe Tunneling. A USB4 hub shall contain an internal PCIe Switch.
11#4	NT	The Device Router in a USB4 hub shall have: An Upstream PCIe Adapter that interfaces to the internal PCIe Switch; For each Downstream Facing Port, a Downstream PCIe Adapter that interfaces to a downstream port of the internal PCIe Switch.
11#5	0	A USB4 device that tunnels PCIe traffic shall contain either an internal PCIe Switch or an internal PCIe Endpoint.
11#6	NT	The Device Router in a USB4 device that supports PCIe tunneling shall have an Upstream PCIe Adapter that interfaces to the internal PCIe Switch or Endpoint.
11.2 Internal PCIe Ports		
11.2#1	TD 11.004 TD 11.005 TD 11.006 TD 11.007 TD 11.009 TD 11.011	Each internal PCIe port that interfaces to a PCIe Adapter shall implement a Physical Layer Logical sub-block, a Data Link Layer, and a Transaction Layer as defined in the PCIe Specification.
11.2.1 PCIe Physical Layer Logical Sub-block		
11.2.1#1	TD 11.002	The Logical sub-block shall update the PCIe configuration registers with the following characteristics: PCIe Gen 1 protocol behavior; Max Link Speed field in the Link Capabilities Register set to 0001b (data rate of 2.5 GT/s only).
11.2.1.1 Encoding		
11.2.1.1#1	NT	The Physical Layer Logical sub-block shall: Not scramble the bits it delivers to the PCIe Adapter Layer; Not de-scramble the bits it receives from the PCIe Adapter Layer, regardless of the Disable Scrambling bit received in the TS Ordered Set.
11.2.1.2 Link Training and Status State Machine (LTSSM)		
11.2.1.2#1	TD 11.007	The LTSSM shall support the L1 state.

11.2.1.2#2	TD 11.003	The LTSSM shall not support the following: Loopback state; L0s state; L1 PM substates; Changes in PCIe link speed; Lane-to-Lane de-skew; Inferring Electrical Idle in states other than L0.
11.2.1.2#3	NT	A PCIe Upstream port in Recovery.idle shall transition to L0 state when it receives a TLP or DLLP. If the port does not receive any TLP or DLLP, it shall transition to the L0 state tRecovery time after it entered the Recovery.idle state.
11.2.1.2#4	NT	A PCIe Downstream Port, shall immediately send UpdateFC after transitioning from L1 to L0.
11.2.1.3 ASPM L1 Entry		
11.2.1.3#1	TD 11.008	The PCIe Upstream Port shall send no more than 10 additional PM_Active_State_Request DLLPs after sending an ACK DLLP for the received PM_Active_State_Nak message.
11.2.1.3#2	NT	After receiving the ACK DLLP for the PM_Active_State_Nak message, the PCIe Downstream Port shall wait 9.5 microseconds as described in the PCIe Specification and shall drop the first 10 PM_Active_State_Request DLLPs it receives. If it receives a TLP or DLLP which is not a PM_Active_State_Request DLLP, it may not drop the next PM_Active_State_Request DLLPs.
11.2.1.4 Clock Tolerance Compensation		
11.2.1.4#1	NT	Clock tolerance compensation shall not be performed.
11.2.1.5 Compliance Mode		
11.2.1.5#1	NT	Compliance Mode shall not be supported.
11.1.1.6 Clock Power Management		
11.2.1.6#1	NT	Clock Power Management shall not be supported.
11.2.2 PCIe Data Link Layer		
11.2.2#1	NT	An internal PCIe Port shall implement a PCIe Data Link Layer as defined in the PCIe Specification.
11.2.3 PCIe Transaction Layer		
11.2.3#1	TD 11.010	Max Payload Size of 128B.
11.2.3#2	TD 11.006	Support the PCIe Latency Tolerance Reporting (LTR) mechanism. The Latency Tolerance Reporting LTR Capability shall be implemented in the PCIe Upstream Port.
11.2.3#3	TD 11.007	Support PCIe hot-add and hot-removal (“hot-plug”).

11.2.3#4	TD 11.008	In a USB4 Hub, the Transaction Layer shall additionally support Access Control Services (ACS).
11.2.3#5	TD 11.009	In a USB4 Hub, the Transaction Layer shall additionally support Flattening Portal Bridge (FPB).
11.2.5 Precision Time Management (PTM) Mechanism		
11.2.5#1	TD 11.012	A USB4 Hub shall support PTM as defined in the PCIe Specification with the modifications in this section.
11.2.5.1 Parameter Generator		
11.2.5.1#1	TD 11.012	The following Routers shall act as a Parameter Generator: A Host Router with its PTM function enabled; A Device Router with its PTM function enabled and the Root Select bit in its PTM Control Register set to 1b.
11.2.5.1#2	NT	A Parameter Generator shall calculate the TMU_to_PTM Parameters as defined in Section 11.1.5.3.1.
11.2.5.1#3	NT	Instead of the PTM Master Time and Propagation Delay fields defined in the PCIe Specification, a Parameter Generator shall include the most recent TMU_to_PTM Parameters in the PTM ResponseD Message as depicted in Figure 11-2.
11.2.5.2 Parameter Consumer		
11.2.5.2#1	NT	A Device Router shall act as Parameter Consumer if its PTM function is enabled and the Root Select bit in its PTM Control Register is set to 0b.
11.2.5.2#2	TD 11.012	When sending a PTM ResponseD Message through a Downstream PCIe Adapter Port, a Parameter Consumer shall use the PTM ResponseD Message format defined in Figure 11-2.
11.2.5.2#3	NT	The TMU_to_PTM Parameters in the ResponseD Message shall be the same as the last TMU_to_PTM Parameters received on the Upstream PCIe Adapter Port.
11.2.5.2#4	TD 11.012	When sending a PTM ResponseD Message to a Native Downstream PCIe Port, a Parameter Consumer shall use the PTM ResponseD Message format defined in the PCIe Specification.
11.2.5.2#5	NT	The Parameter Consumer shall calculate the PTM Master Time for the PTM ResponseD Message as defined in Section 11.2.5.3.2.
11.1 PCIe Adapter Layer		
11.1.1 Encapsulation		

11.1.1#1	BCP	The PCIe Adapter Layer shall encapsulate the following PCIe constructs in Tunneled Packets: Transaction Layer Packets (TLP); Data Link Layer Packets (DLLP); Ordered Sets; Out-of-band events.
11.1.1#2	TBD	A PCIe Adapter Layer shall not encapsulate Idle data Symbols into Tunneled Packets.
11.1.1#3	BCP	A TLP or a DLLP shall fit into a single Tunneled Packet
11.1.1#4	BCP	A Tunneled Packet may contain a single TLP or DLLP, or it may contain a DLLP followed by a TLP or DLLP. It shall not contain any other TLP/DLLP combinations.
11.1.1#5	BCP	Each Ordered Set shall be encapsulated into a separate Tunneled Packet.
11.1.1#6	BCP	Each PCIe out-of-band event shall be encapsulated into a separate Tunneled Packet.
11.1.1#7	BCP	The order of bytes and bits in the Tunneled Packet shall be identical to the original PCIe construct. The least-significant byte of the encapsulated construct is mapped to B0 in the Tunneled Packet Payload (see Figure 4-17). Bit 7 in each byte of the encapsulated construct is mapped to bit 7 in respective byte of the Tunneled Packet Payload.
11.1.1#8	BCP	Table 11-2 defines the PDF values that shall be used for each type of PCIe construct.
11.1.1#9	NT	If a PCIe Adapter Port receives a Tunneled Packet with a Rsvd PDF value, it shall discard the Tunneled Packet and shall not send any Packets in response.
11.1.1.1 PCIe TLP and DLLP		
11.1.1.1#1	NT	A PCIe Adapter Port shall not discard a PCIe TLP or DLLP due to lack of credits in the USB4 fabric. When credits are not available, the Router shall queue the PCIe TLP and shall transport it once sufficient credits become available.
11.1.1.1#2	NT	When a PCIe Adapter Layer receives a Tunneled Packet with a pre-header that does not match any of the pre-headers defined in this section, it shall discard the packet and report the mismatch as a PCIe Receiver Error to the internal PCIe Port.
11.1.1.1.1 TLP Encapsulation		
11.1.1.1.1#1	NT	A PCIe Adapter Port shall not send a Tunneled Packet for the following: A Nullified TLP; A Truncated TLP; A Truncated DLLP.

11.1.1.1.1#2	BCP	As shown in Figure 11-4, before encapsulation into a Tunneled Packet, a PCIe Adapter Layer shall: 1. Truncate a TLP by removing the STP Symbol, four leading Reserved bits, and the END Symbol; 2. Add the TLP pre-header defined in Table 11-3.
11.1.1.1.2 DLLP Encapsulation		
11.1.1.1.2#1	BCP	Before encapsulating a DLLP into a Tunneled Packet, a PCIe Adapter Layer shall: 1. Truncate a DLLP by removing the SDP Symbol and the END Symbol; 2. Add a DLLP pre-header of 0FACH to a DLLP as shown in Figure 11-6.
11.1.1.1.3 Mixed TLP/DLLP Encapsulation		
11.1.1.1.3#1	BCP	When a Tunneled Packet contains a DLLP followed by a TLP or DLLP, each DLLP or TLP shall contain its own pre-header.
11.1.1.2 PCIe Ordered Sets		
11.1.1.2.1 Training Sequence (TS) Ordered Sets		
11.1.1.2.1#1	TD 11.005 TD 11.006	When a PCIe Adapter Layer receives one or more identical TS1 Ordered sets in a row from the internal PCIe Port, it shall transmit 16 copies of the TS1 Ordered set before it transmits another Tunneled PCIe Packet. The PCIe Adapter Layer may transmit more than 16 TS1 Ordered sets before transmitting a Tunneled PCIe Packet.
11.1.1.2.1#2	TD 11.005 TD 11.006	When a PCIe Adapter Layer receives one or more identical TS2 Ordered sets in a row from the internal PCIe Port, it shall transmit 16 copies of the TS2 Ordered set before it transmits another Tunneled PCIe Packet. The PCIe Adapter Layer may transmit more than 16 TS2 Ordered sets before transmitting a Tunneled PCIe Packet.
11.1.1.2.1#3	TD 11.005 TD 11.006	A PCIe Adapter Layer shall only transmit TS Ordered Sets that target Lane 0. TS Ordered Sets that target a non-zero Lane shall be discarded and shall not be send over the USB4 fabric.
11.1.1.2.1#4	TD 11.005 TD 11.006	A PCIe Adapter Layer shall modify a TS Ordered Set as defined in Table 11-4.
11.1.1.2.1#5	NT	Upon receiving a TS Ordered Set from the Transport Layer, a PCIe Adapter Layer shall transfer the TS Ordered Set to the internal PCIe Port.
11.1.1.2.2 Electrical Idle Ordered Sets (EIOS)		
11.1.1.2.2#1	TD 11.005 TD 11.007	When a PCIe Adapter Layer receives an Electrical Idle Ordered Set (EIOS) from the internal PCIe Port, it shall send two consecutive EIOS Tunneled Packets over the USB4 fabric.

11.1.1.2.2#2	TD 11.005 TD 11.007	An EIOS shall be encapsulated in a Tunneled Packet with payload as defined in Table 11-5.
11.1.1.2.2#3	NT	A PCIe Adapter Layer that receives an EIOS Tunneled Packet shall: 1. Transfer the EIOS to the internal PCIe Port; 2. Indicate Rx Electrical Idle to the internal PCIe Port.
11.1.1.3 Electrical Idle State		
11.1.1.3#1	TD 11.007	Upon detecting that a PCIe Physical Layer Logical sub-block is in Electrical Idle state, a PCIe Adapter Layer shall send at least 3 Electrical Idle State Tunneled Packets.
11.1.1.3#2	TD 11.007	The payload for an Electrical Idle State Tunneled Packet shall consist of one DW that contains a value of 0000 0000h.
11.1.1.3#3	NT	A PCIe Adapter Layer that receives an Electrical Idle State Tunneled Packet shall indicate Rx Electrical Idle to the internal PCIe Port.
11.1.1.3#4	NT	When a PCIe Adapter Layer receives a Tunneled Packet that is not an Electrical Idle State Tunneled Packet or an EIOS Tunneled Packet, it shall stop indicating Rx Electrical Idle to the internal PCIe Port.
11.1.1.4 PERST		
11.1.1.4.1 PERST Tunneled Packets		
11.1.1.4.1#1	NT	A Router shall send PERST Active and PERST Inactive packets only from a Downstream PCIe Adapter Port.
11.1.1.4.1#2	TD 11.014	The payload for a PERST Active Tunneled Packet and a PERST Inactive Tunneled Packet shall consist of one DW that contains a value of 0000 0000h.
11.1.1.4.2 PERST Activation in a Host Router		
11.1.1.4.2#1	TD 11.014	Upon detecting an assertion of PERST# on a Downstream PCIe Adapter, a Host Router shall: 1. Discard any queued Tunneled Packet in the PCIe Adapter Layer; 2. Send at least three PERST Active Tunneled Packets on the Downstream PCIe Adapter if its Path Enable bit is set to 1b.
11.1.1.4.3 PERST Activation in a Device Router		
11.1.1.4.3#1	TBD	When a Device Router enters Uninitialized Unplugged state, it shall assert PERST# on its internal PCIe upstream port.

11.1.1.4.3#2	TD 11.014	When a Device Router receives a PERST Active Tunneled Packet or the Path Enable bit in the Upstream PCIe Adapter is set to 0b , it shall: 1. Discard any Tunneled Packets that are queued in a PCIe Adapter Layer; 2. Send at least 3 PERST Active Tunneled Packets on all Downstream PCIe Adapter Ports that have the Path Enable bit set to 1b. 3. Assert PERST# on its internal PCIe Upstream Port. [Previously 11.1.1.4.2.1#2]
11.1.1.4.3#3	NT	While PERST# is asserted, a Downstream PCIe Adapter Layer shall discard any PCIe Tunneled Packets it receives. [Previously 11.1.1.4.2.1#3]
11.1.1.4.4 PERST Inactivation in a Host Router		
11.1.1.4.4#1	TD 11.014	Upon detecting a de-assertion of PERST# on a Downstream PCIe Adapter , a Host Router shall send at least 3 PERST Inactive Tunneled Packets on the Downstream PCIe Adapter if its Path Enable bit is set to 1b.[Previously 11.1.1.4.2.2#1]
11.1.1.4.5 PERST Inactivation in a Device Router		
11.1.1.4.5#1	TD 11.014	After receiving a PERST Active Tunneled Packet or after the Path Enable bit the Upstream PCIe Adapter is set from 0b to 1b , if a Device Router receives any PCIe Tunneled Packet other than a PERST Active Tunneled Packet on its Upstream PCIe Adapter Port, it shall: Send at least 3 PERST Inactive Tunneled Packets on all Downstream PCIe Adapter Ports that have the Path Enable bit set to 1b; De-assert PERST# its internal PCIe upstream port. [Previously 11.1.1.4.2.2#2]
11.1.1.4.5#2	NT	After PERST# is de-asserted, a Downstream PCIe Adapter Layer shall not forward to the internal PCIe Port any Ordered Sets, packets, or events that were received before or during PERST# assertion. [Previously 11.1.1.4.2.2#3]
11.1.2 USB4 Hot-Plug		
11.1.2#1	TD 11.014 TD 11.020	When a Device Router is hot-plugged, the Upstream Adapter Port in the hot-plugged Router shall maintain the internal PCIe Port in PCIe Warm Reset.
11.1.2#2	TD 11.017 TD 11.020	The Device Router shall maintain the Warm Reset until either a PERST Inactive Tunneled Packet or a PCIe TS Ordered Set is received by the Upstream Adapter Port.
11.3 Paths		
11.3#1	NT	A PCIe Adapter Layer shall put HopID = 8 in the header of an outgoing Tunneled Packet before handing it off to the Transport Layer for routing
11.3.1 Path Set-Up		

11.3.1#1	TBD	Before setting up a Path, the Router does not indicate in-band presence to the Internal PCIe Port. The internal PCIe Port LTSSM is in the Detect state.
11.3.1#2		Deprecated.
11.3.1#3	TBD	When the Path Enable bit is set to 1b, a Router shall indicate in-band presence to the internal PCIe Port.
11.3.1#4	TBD	The PCIe Adapter Layer shall also enable sending of PCIe Tunneled Packets to the Transport Layer.
11.3.1#5	NT	When an internal PCIe Port detects an in-band presence, it shall: Transition its LTSSM to the Polling state; Generate a PCIe interrupt to indicate a hot plug event to software.
11.3.2 Path Tear-Down		
11.3.2#1	TD 11.020	When a Router detects a disconnect event on a Downstream Facing USB4 Port, it shall: Set the Path Enable bit to 0b in the PCIe Adapter Port Configuration Capability of the PCIe Adapter Port associated with the USB4 Port via the Router's Routing Tables.
11.3.2#2	TD 11.020	When the Path Enable bit is set to 0b in its PCIe Adapter Configuration Capability, a PCIe Adapter shall: Disable sending of PCIe Tunneled Packets from the PCIe Adapter Layer to the Transport Layer; If the PCIe Adapter is a Downstream PCIe Adapter, clear the In-band Presence 1 indication to the internal PCIe port; If the PCIe Adapter is an Upstream PCIe Adapter, drive PERST# as defined in Section 11.1.1.4.3.
11.3.2#3	NT	When an internal PCIe Port detects that the in-band presence indicator is cleared, it shall: Transition its LTSSM to the Recovery state followed by transition to the Detect state. It is recommended that the LTSSM not wait the full amount of time defined in the PCIe Specification before transitioning to the Detect state; Generate a PCIe interrupt to indicate a hot removal event to software.

Ver. 2 Assertions

The following Table presents the Chapter 11 assertions from the USB4 Ver. 2 Specification.

Assertion #	Test Name	Assertion Description
11 PCI Express Tunneling		
11#1	Deprecated	A USB4 host that tunnels PCIe traffic does one of the following: Incorporate an internal PCIe Switch; Connect to a Root Complex via Root Ports.
11#2	TD 11.1	The Host Router in a USB4 host that supports PCIe Tunneling shall have one Downstream PCIe Adapter per Downstream Facing Port. Each Downstream PCIe Adapter shall interface to a downstream port of the internal PCIe Switch or Root Complex.
11#3	TD 11.1	A USB4 hub shall support PCIe Tunneling. A USB4 hub shall contain an internal PCIe Switch.
11#4	TD 11.1	The Device Router in a USB4 hub shall have: An Upstream PCIe Adapter that interfaces to the internal PCIe Switch; For each Downstream Facing Port, a Downstream PCIe Adapter that interfaces to a downstream port of the internal PCIe Switch.
11#5	TD 11.1	A USB4 device that tunnels PCIe traffic shall contain either an internal PCIe Switch or an internal PCIe Endpoint.
11#6	TD 11.1	The Device Router in a USB4 device that supports PCIe tunneling shall have an Upstream PCIe Adapter that interfaces to the internal PCIe Switch or Endpoint.
11.1 PCIe Adapter Layer		
11.1.1 Encapsulation		
11.1.1#1	TD 11.13 BCP	The PCIe Adapter Layer shall encapsulate the following PCIe constructs in Tunneled Packets: Transaction Layer Packets (TLP); Data Link Layer Packets (DLLP); Ordered Sets; Out-of-band events.
11.1.1#2		A PCIe Adapter Layer shall not encapsulate Idle Data Symbols into Tunneled Packets.
11.1.1#3		A PCIe Adapter Layer shall follow the rules below when encapsulating a PCIe construct into a Tunneled Packet: TLPs and DLLPs shall be encapsulated as defined in Section 11.1.1.1.3.
11.1.1#4	TD 11.13 BCP	A PCIe Adapter Layer shall follow the rules below when encapsulating a PCIe construct into a Tunneled Packet: Each Ordered Set shall be encapsulated into a separate Tunneled Packet.

11.1.1#5	TD 11.13 BCP	A PCIe Adapter Layer shall follow the rules below when encapsulating a PCIe construct into a Tunneled Packet: Each PCIe out-of-band event shall be encapsulated into a separate Tunneled Packet.
11.1.1#6		A PCIe Adapter Layer shall follow the rules below when encapsulating a PCIe construct into a Tunneled Packet: The order of bytes and bits in the Tunneled Packet shall be identical to the original PCIe construct.
11.1.1#7		The PDF field in a Tunneled Packet identifies the type of PCIe construct contained therein. Table 11-1 defines the PDF values that shall be used for each type of PCIe construct.
11.1.1#8		If a PCIe Adapter receives a Tunneled Packet with a Rsvd PDF value, it shall discard the Tunneled Packet and shall not send any Packets in response.
11.1.1.1 PCIe TLP and DLLP		
11.1.1.1#1		When a PCIe Adapter Layer receives a Tunneled Packet with a pre-header that does not match any of the pre-headers defined in this section, it shall discard the packet and report the mismatch as a PCIe Receiver Error to the Internal PCIe Port.
11.1.1.1.1 Tunneled Packet Payload for TLP		
11.1.1.1.1#1		As shown in Figure 11 1, before encapsulation into a Tunneled Packet, a PCIe Adapter Layer shall: 1.Truncate a TLP by removing the STP Symbol, four leading Reserved bits, and the END or EDB Symbol.
11.1.1.1.1#2		As shown in Figure 11 1, before encapsulation into a Tunneled Packet, a PCIe Adapter Layer shall: 2.Add the TLP Pre-Header defined in Table 11 2.
11.1.1.1.2 Tunneled Packet Payload for DLLP		
11.1.1.1.2#1		Before encapsulating a DLLP into a Tunneled Packet, a PCIe Adapter Layer shall: 1. Truncate a DLLP by removing the SDP Symbol and the END Symbol.
11.1.1.1.2#2		Before encapsulating a DLLP into a Tunneled Packet, a PCIe Adapter Layer shall: 2. Add a DLLP Pre-Header of 0FACH to a DLLP as shown in Figure 11-3
11.1.1.1.3 DLLP and TLP Encapsulation		
11.1.1.1.3#1	TD11.13	A PCIe Adapter Layer shall support all the following options for encapsulating DLLPs and TLPs into Tunneled Packets: Single TLP.

11.1.1.1.3#2	TD11.13	A PCIe Adapter Layer shall support all the following options for encapsulating DLLPs and TLPs into Tunneled Packets: 1 to N DLLPs: the <i>Extended Encapsulation</i> bit in the PCIe Adapter Configuration Capability is set to 0b, N=2; When the <i>Extended Encapsulation</i> bit in the PCIe Adapter Configuration Capability is set to 1b, N=3.
11.1.1.1.3#3	TD11.13	A PCIe Adapter Layer shall support all the following options for encapsulating DLLPs and TLPs into Tunneled Packets: 1 to M DLLPs followed by a single TLP: When the <i>Extended Encapsulation</i> bit in the PCIe Adapter Configuration Capability is set to 0b, M=1; When the <i>Extended Encapsulation</i> bit in the PCIe Adapter Configuration Capability is set to 1b, M=2.
11.1.1.1.3#4	TD11.13 TD11.100	If the total payload size of the encapsulated DLLPs and TLP is 252 bytes or less, the PCIe Adapter Layer shall encapsulate the DLLPs and/or TLP into a single Tunneled Packet with PDF = 3h. A nullified TLP shall be discarded and shall not be encapsulated.
11.1.1.1.3#5	TD11.13	If the total payload size of the encapsulated DLLPs and TLP exceeds 252 bytes, the PCIe Adapter Layer shall encapsulate the DLLPs and TLP into multiple Tunneled Packets according to the following rules: All encapsulated DLLPs shall fit into the first Tunneled Packet.
11.1.1.1.3#6	TD11.13	If the total payload size of the encapsulated DLLPs and TLP exceeds 252 bytes, the PCIe Adapter Layer shall encapsulate the DLLPs and TLP into multiple Tunneled Packets according to the following rules: The encapsulated TLP shall be segmented into multiple Tunneled Packets. All Tunneled Packets, with the possible exception of the last, shall contain 252B of payload. The last Tunneled Packet shall contain up to 252B of payload.
11.1.1.1.3#7	TD11.13 BCP	If the total payload size of the encapsulated DLLPs and TLP exceeds 252 bytes, the PCIe Adapter Layer shall encapsulate the DLLPs and TLP into multiple Tunneled Packets according to the following rules: The first Tunneled Packet shall be assigned a PDF=3h.
11.1.1.1.3#8	TD11.13 BCP	If the total payload size of the encapsulated DLLPs and TLP exceeds 252 bytes, the PCIe Adapter Layer shall encapsulate the DLLPs and TLP into multiple Tunneled Packets according to the following rules: The following Tunneled Packets shall be assigned a PDF=4h.
11.1.1.1.3#9		If extended encapsulation is enabled: If the total payload size of the encapsulated DLLPs and TLP exceeds 252 bytes, the PCIe Adapter Layer shall encapsulate the DLLPs and TLP into multiple Tunneled Packets according to the following rules:
11.1.1.1.3#10	TD11.100	If the total payload size of the encapsulated DLLPs and TLP exceeds 252 bytes, the PCIe Adapter Layer shall encapsulate the DLLPs and TLP into multiple Tunneled Packets according to the following rules: A nullified TLP may be discarded by the transmitting Router or may be transmitted over the tunnel. If the TLP is transmitted, the last Tunneled Packet for that TLP shall be assigned a PDF=7h as an EnD Bad (EDB) indication.

11.1.1.2 PCIe Ordered Sets		
11.1.1.2#1		A PCIe Adapter Layer that receives a TS Ordered Set (TS1 or TS2) or an Electrical Idle Ordered Set (EIOS) from the Internal PCIe Port shall transfer the Ordered Set to the Transport Layer as defined in the sections below.
11.1.1.2#2		All other Ordered Sets shall be discarded and shall not be transferred to the Transport Layer.
11.1.1.2.1 Training Sequence (TS) Ordered Sets		
11.1.1.2.1#1	TD 11.005	Transmitter rules: When a PCIe Adapter Layer receives one or more identical TS1 Ordered sets in a row from the Internal PCIe Port, it shall transmit 16 copies of the TS1 Ordered set before it transmits another Tunneled PCIe Packet.
11.1.1.2.1#2	TD 11.006	Transmitter rules: When a PCIe Adapter Layer receives one or more identical TS2 Ordered sets in a row from the Internal PCIe Port, it shall transmit 16 copies of the TS2 Ordered set before it transmits another Tunneled PCIe Packet.
11.1.1.2.1#3	TD 11.005	Transmitter rules: A PCIe Adapter Layer shall only transmit TS Ordered Sets that target Lane 0. TS Ordered Sets that target a non-zero Lane shall be discarded and shall not be send over the USB4 Fabric.
11.1.1.2.1#4	TD 11.006	Transmitter rules: A PCIe Adapter Layer shall modify a TS Ordered Set as defined in Table 11-3.
11.1.1.2.1#5	NT	Receiver rules: Upon receiving a TS Ordered Set from the Transport Layer, a PCIe Adapter Layer shall transfer the TS Ordered Set to the Internal PCIe Port.
11.1.1.2.2 Electrical Idle Ordered Sets (EIOS)		
11.1.1.2.2#1	TD 11.005 TD 11.007	When a PCIe Adapter Layer receives an Electrical Idle Ordered Set (EIOS) from the Internal PCIe Port, it shall send two consecutive EIOS Tunneled Packets over the USB4 Fabric.
11.1.1.2.2#2	TD 11.005 TD 11.007	An EIOS shall be encapsulated in a Tunneled Packet with payload as defined in Table 11 4.
11.1.1.2.2#3	NT	A PCIe Adapter Layer that receives an EIOS Tunneled Packet shall: 1.Transfer the EIOS to the Internal PCIe Port; 2.Indicate Rx Electrical Idle to the Internal PCIe Port.
11.1.1.3 Electrical Idle State		
11.1.1.3#1	TD 11.007	Upon detecting that a PCIe Physical Layer Logical sub-block is in Electrical Idle state, a PCIe Adapter Layer shall send at least 3 Electrical Idle State Tunneled Packets.

11.1.1.3#2	TD 11.007	The payload for an Electrical Idle State Tunneled Packet shall consist of one DW that contains a value of 0000 0000h.
11.1.1.3#3	NT	A PCIe Adapter Layer that receives an Electrical Idle State Tunneled Packet shall indicate Rx Electrical Idle to the Internal PCIe Port.
11.1.1.3#4	NT	When a PCIe Adapter Layer receives a Tunneled Packet that is not an Electrical Idle State Tunneled Packet or an EIOS Tunneled Packet, it shall stop indicating Rx Electrical Idle to the Internal PCIe Port.
11.1.1.4 PERST		
11.1.1.4.1 PERST Tunneled Packets		
11.1.1.4.1#1	NT	A Router shall send PERST Active and PERST Inactive packets only from a Downstream PCIe Adapter.
11.1.1.4.1#2	TD 11.014	The payload for a PERST Active Tunneled Packet and a PERST Inactive Tunneled Packet shall consist of one DW that contains a value of 0000 0000h.
11.1.1.4.2 PERST Activation in a Host Router		
11.1.1.4.2#1		Upon detecting an assertion of PERST# on a Downstream PCIe Adapter, a Host Router shall: 1. Discard any queued Tunneled Packet in the PCIe Adapter Layer.
11.1.1.4.2#2		Upon detecting an assertion of PERST# on a Downstream PCIe Adapter, a Host Router shall: 2. Send at least three PERST Active Tunneled Packets on the Downstream PCIe Adapter if its Path Enable bit is set to 1b.
11.1.1.4.3 PERST Activation in a Device Router		
11.1.1.4.3#1		When a Device Router enters the Uninitialized Unplugged state, it shall assert PERST# on its internal PCIe upstream port.
11.1.1.4.3#2		When a Device Router receives a PERST Active Tunneled Packet, or the Path Enable bit in the Upstream PCIe Adapter is set to 0b, it shall: 1. Discard any Tunneled Packets that are queued in a PCIe Adapter Layer.
11.1.1.4.3#3		When a Device Router receives a PERST Active Tunneled Packet, or the Path Enable bit in the Upstream PCIe Adapter is set to 0b, it shall: 2. Send at least 3 PERST Active Tunneled Packets on all Downstream PCIe Adapters that have the Path Enable bit set to 1b.
11.1.1.4.3#4		When a Device Router receives a PERST Active Tunneled Packet, or the Path Enable bit in the Upstream PCIe Adapter is set to 0b, it shall: 3. Assert PERST# on its internal PCIe upstream port.

11.1.1.4.3#5		While PERST# is asserted, a Downstream PCIe Adapter Layer shall discard any received PCIe Tunneled Packets.
11.1.1.4.3#6		The Adapter Layer shall not send any PCIe Tunneled Packets except for the PERST Active Tunneled Packets.
11.1.1.4.4 PERST Inactivation in a Host Router		
11.1.1.4.4#1		Upon detecting a de-assertion of PERST# on a Downstream PCIe Adapter, a Host Router shall send at least 3 PERST Inactive Tunneled Packets on the Downstream PCIe Adapter if its Path Enable bit is set to 1b.
11.1.1.4.5 PERST Inactivation in a Device Router		
11.1.1.4.5#1		After receiving a PERST Active Tunneled Packet, or after the Path Enable bit in the Upstream PCIe Adapter changes from 0b to 1b, if a Device Router receives any PCIe Tunneled Packet other than a PERST Active Tunneled Packet on its Upstream PCIe Adapter, it shall: 1. Send at least 3 PERST Inactive Tunneled Packets on all Downstream PCIe Adapters that have the Path Enable bit set to 1b.
11.1.1.4.5#2		After receiving a PERST Active Tunneled Packet, or after the Path Enable bit in the Upstream PCIe Adapter changes from 0b to 1b, if a Device Router receives any PCIe Tunneled Packet other than a PERST Active Tunneled Packet on its Upstream PCIe Adapter, it shall: 2. De-assert PERST# on its internal PCIe upstream port .
11.1.1.4.5#3		After PERST# is de-asserted, a Downstream PCIe Adapter Layer shall not forward to the Internal PCIe Port any Ordered Sets, packets, or events that were received before or during PERST# assertion.
11.1.2 USB4 Hot-Plug		
11.1.2#1	TD 11.14 TD 11.19	When a Device Router is hot-plugged, the Upstream PCIe Adapter in the hot-plugged Router shall maintain the Internal PCIe Port in PCIe Warm Reset.
11.1.2#2	TD 11.19	The Device Router shall maintain the Warm Reset until either a PERST Inactive Tunneled Packet or a PCIe TS Ordered Set is received by the Upstream PCIe Adapter.
11.1.3 Flow Control		
11.1.3#1		A PCIe Adapter shall not discard a PCIe TLP or DLLP due to lack of credits in the USB4 Link.
11.1.3#2		When credits are not available, the Router shall queue the PCIe TLP and shall transport it once sufficient credits become available.

11.1.3#3		When credits are not available, a Router may hold off creation of new DLLPs.
11.1.4 PCIe Wake		
11.1.4.1 Router is in the Sleep State		
11.1.4.1#1		A Device Router that detects a PCIe Wake event from any connected PCIe Endpoint or Switch, and the Sleep Ready bit in Router Configuration Space is set to 1b shall process the wake as defined in Section 4.5.
11.1.4.1#2		If a PCIe wake event happens after the Sleep Ready bit is set to 1b but before the Device Router is in sleep state, the Device Router shall wait for entry to sleep state and then process the wake as defined in Section 4.5.
11.1.4.2 Router is in the Enumerated state		
11.1.4.2#1	TD11.101	A Device Router in the Enumerated state shall send a Notification Packet upstream with the Event Code = PCIE_WAKE (see Section 6.5) when all the following are true: The Upstream PCIe Adapter detects a PCIe Wake event from the connected PCIe Endpoint or Switch; The Enumerated State PCIe Wake bit in Router Configuration Space is set to 1b; The Sleep Ready bit in Router Configuration Space is set to 0b.
11.1.4.2#2		If the Enter Sleep bit is set to 1b while the Device Router is processing a wake event and a Notification Packet has not been sent yet, the Router shall finish processing the wake event (including sending a Notification Packet and receiving a Notification Acknowledgement Packet) before it sets the Sleep Ready bit to 1b.
11.1.4.2#3	TD11.101	A Host Router that receives a Notification Packet with Event Code = PCIE_WAKE shall: Generate a PCIe wake indication to the host system. The mechanism for waking the host system is outside the scope of this specification.
11.1.4.2#4	TD11.101	A Host Router that receives a Notification Packet with Event Code = PCIE_WAKE shall: Forward the Notification Packet to the Connection Manager.
11.2 Internal PCIe Ports		
11.2#1	TD 11.004 TD 11.005 TD 11.006 TD 11.007 TD 11.009 TD 11.011	Each internal PCIe port that interfaces to a PCIe Adapter shall implement a Physical Layer Logical sub-block, a Data Link Layer, and a Transaction Layer as defined in the PCIe Specification.

11.2.1 PCIe Physical Layer Logical Sub-block		
11.2.1#1	TD 11.002	The Logical sub-block shall update the PCIe configuration registers with the following characteristics: PCIe Gen 1 protocol behavior; Max Link Speed field in the Link Capabilities Register set to 0001b (data rate of 2.5 GT/s only).
11.2.1.1 Encoding		
11.2.1.1#1	NT	The Physical Layer Logical sub-block shall: Not scramble the bits it delivers to the PCIe Adapter Layer; Not de-scramble the bits it receives from the PCIe Adapter Layer, regardless of the Disable Scrambling bit received in the TS Ordered Set.
11.2.1.2 Link Training and Status State Machine (LTSSM)		
11.2.1.2#1	TD 11.7	The LTSSM shall support the L1 state.
11.2.1.2#2	TD 11.5	The LTSSM shall not support the following: Loopback state; L0s state; L1 PM substates; Changes in PCIe link speed; Lane-to-Lane de-skew; Inferring Electrical Idle in states other than L0.
11.2.1.2#3	NT	A PCIe Upstream port in Recovery.idle shall transition to L0 state when it receives a TLP or DLLP. If the port does not receive any TLP or DLLP, it shall transition to the L0 state tRecovery time after it entered the Recovery.idle state.
11.2.1.2#4	NT	A PCIe Downstream Port, shall immediately send UpdateFC after transitioning from L1 to L0.
11.2.1.3 ASPM L1 Entry		
11.2.1.3#1	TD 11.8	The PCIe Upstream Port shall send no more than 10 additional PM_Active_State_Request DLLPs after sending an ACK DLLP for the received PM_Active_State_Nak message.
11.2.1.3#2	NT	After receiving the ACK DLLP for the PM_Active_State_Nak message, the PCIe Downstream Port shall wait 9.5 microseconds as described in the PCIe Specification and shall drop the first 10 PM_Active_State_Request DLLPs it receives. If it receives a TLP or DLLP which is not a PM_Active_State_Request DLLP, it may not drop the next PM_Active_State_Request DLLPs.
11.2.1.4 Clock Tolerance Compensation		
11.2.1.4#1	NT	Clock tolerance compensation shall not be performed.
11.2.1.5 Compliance Mode		
11.2.1.5#1	NT	Compliance Mode shall not be supported.

11.2.1.6 Clock Power Management		
11.2.1.6#1	NT	Clock Power Management shall not be supported.
11.2.2 PCIe Data Link Layer		
11.2.2#1	NT	An internal PCIe Port shall implement a PCIe Data Link Layer as defined in the PCIe Specification.
11.2.3 PCIe Transaction Layer		
11.2.3#1	TD 11.010	Deprecated.
11.2.3#2	TD 11.006	Support the PCIe Latency Tolerance Reporting (LTR) mechanism. The Latency Tolerance Reporting LTR Capability shall be implemented in the PCIe Upstream Port.
11.2.3#3	TD 11.007	Support PCIe hot-add and hot-removal (“hot-plug”).
11.2.3#4	TD 11.008	In a USB4 Hub, the Transaction Layer shall additionally support Access Control Services (ACS).
11.2.3#5	TD 11.009	In a USB4 Hub, the Transaction Layer shall additionally support Flattening Portal Bridge (FPB).
11.2.4 Precision Time Management (PTM) Mechanism		
11.2.4#1	TD 11.012	A USB4 Hub shall support PTM as defined in the PCIe Specification with the modifications in this section. [Previously 11.2.5#1]
11.2.4#2		If a USB4 Host supports PTM, it shall do so as defined in this section.
11.2.4.1 Parameter Generator		
11.2.4.1#1	TD 11.012	The following Routers shall act as a Parameter Generator: A Host Router with its PTM function enabled; A Device Router with its PTM function enabled and the Root Select bit in its PTM Control Register set to 1b. [Previously 11.2.5.1#1]
11.2.4.1#2	NT	A Parameter Generator shall calculate the TMU_to_PTM Parameters as defined in Section 11.1.5.3.1. [Previously 11.2.5.1#2]
11.2.4.1#3	NT	Instead of the PTM Master Time and Propagation Delay fields defined in the PCIe Specification, a Parameter Generator shall include the most recent TMU_to_PTM Parameters in the PTM ResponseD Message as depicted in Figure 11-2. [Previously 11.2.5.1#3]

11.2.4.2 Parameter Consumer		
11.2.4.2#1	NT	A Device Router shall act as Parameter Consumer if its PTM function is enabled and the Root Select bit in its PTM Control Register is set to 0b. [Previously 11.2.5.2#1]
11.2.4.2#2	TD 11.012	When sending a PTM ResponseD Message through a Downstream PCIe Adapter Port, a Parameter Consumer shall use the PTM ResponseD Message format defined in Figure 11-2. [Previously 11.2.5.2#2]
11.2.4.2#3	NT	The TMU_to_PTM Parameters in the ResponseD Message shall be the same as the last TMU_to_PTM Parameters received on the Upstream PCIe Adapter Port. [Previously 11.2.5.2#3]
11.2.4.2#4	TD 11.012	When sending a PTM ResponseD Message to a Native Downstream PCIe Port, a Parameter Consumer shall use the PTM ResponseD Message format defined in the PCIe Specification. [Previously 11.2.5.2#4]
11.2.4.2#5	NT	The Parameter Consumer shall calculate the PTM Master Time for the PTM ResponseD Message as defined in Section 11.2.4.3.2. [Previously 11.2.5.2#5]
11.2.4.3 PTM Calculations		
11.2.4.3.1 TMU_to_PTM Parameters		
11.2.4.3.1#1		To compensate for any quantization error, a Parameter Generator shall calculate the TMU_to_PTM Parameters as follows: 1. Calculate the ideal 64-bit parameters; 2. Calculate the ptm_error at ptm1 point using the 32 bits representation of the slope; 3. Assign the TMU to PTM Parameters.
11.2.4.3.2 PTM Master Time Reconstruction		
11.2.4.3.2#1		A Parameter Consumer shall reconstruct the PTM Master Time as follows: $PTM_Master_Time(t) = TMU_to_PTM_A * TMU_time(t) + TMU_to_PTM_B$.
11.2.5 Timing Parameters		
11.3 Paths		
11.3#1	NT	A PCIe Adapter Layer shall put HopID = 8 in the header of an outgoing Tunneled Packet before handing it off to the Transport Layer for routing
11.3.1 Path Set-Up		
11.3.1#1	TBD	Before setting up a Path, the Router does not indicate in-band presence to the Internal PCIe Port. The internal PCIe Port LTSSM is in the Detect state.

11.3.1#2		Deprecated.
11.3.1#3	TBD	When the Path Enable bit is set to 1b, a Router shall indicate in-band presence to the internal PCIe Port.
11.3.1#4	TBD	The PCIe Adapter Layer shall also enable sending of PCIe Tunneled Packets to the Transport Layer.
11.3.1#5	NT	When an internal PCIe Port detects an in-band presence, it shall: Transition its LTSSM to the Polling state; Generate a PCIe interrupt to indicate a hot plug event to software.
11.3.2 Path Teardown		
11.3.2#1	TD 11.020	Deprecated.
11.3.2#2	TD 11.020	When the Path Enable bit is set to 0b in its PCIe Adapter Configuration Capability (including a DFP disconnect - see Section 4.4.5.2.1), a PCIe Adapter shall: Disable sending of PCIe Tunneled Packets from the PCIe Adapter Layer to the Transport Layer; If the PCIe Adapter is a Downstream PCIe Adapter, clear the In-band Presence 1 indication to the internal PCIe port; If the PCIe Adapter is an Upstream PCIe Adapter, drive PERST# t as defined in Section 11.1.1.4.2; Set the <i>Extended Encapsulation</i> bit to its default value.
11.3.2#3	NT	When an internal PCIe Port detects that the in-band presence indicator is cleared, it shall: Transition its LTSSM to the Recovery state followed by transition to the Detect state. It is recommended that the LTSSM not wait the full amount of time defined in the PCIe Specification before transitioning to the Detect state; Generate a PCIe interrupt to indicate a hot removal event to software.

Test Setups

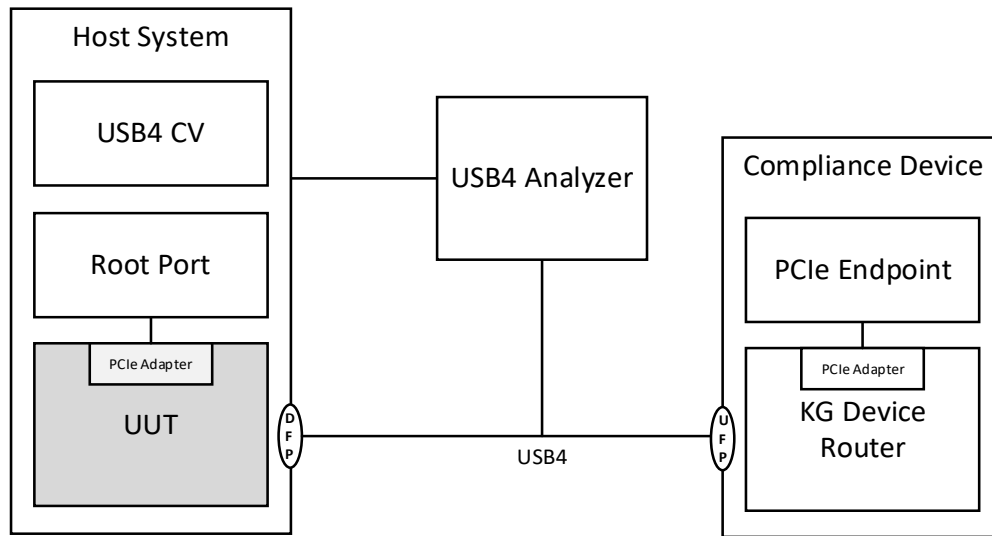
Host

This section describes the test setup for a Host Router.

AN_HOST_DFP1—PCIE_01

- Vendor provides the host system for the UUT with:
 - USB4 CV installed
 - The relevant PCIe-related capabilities (PTM, ASPM, etc.) enabled in the BIOS/OS as required for testing
- A KG USB4 Device with a known PCIe endpoint is connected downstream.
- A USB4 Analyzer is connected between the UUT and KG USB4 Device.

Note: Some tests require the use of an active cable on the USB4 Link

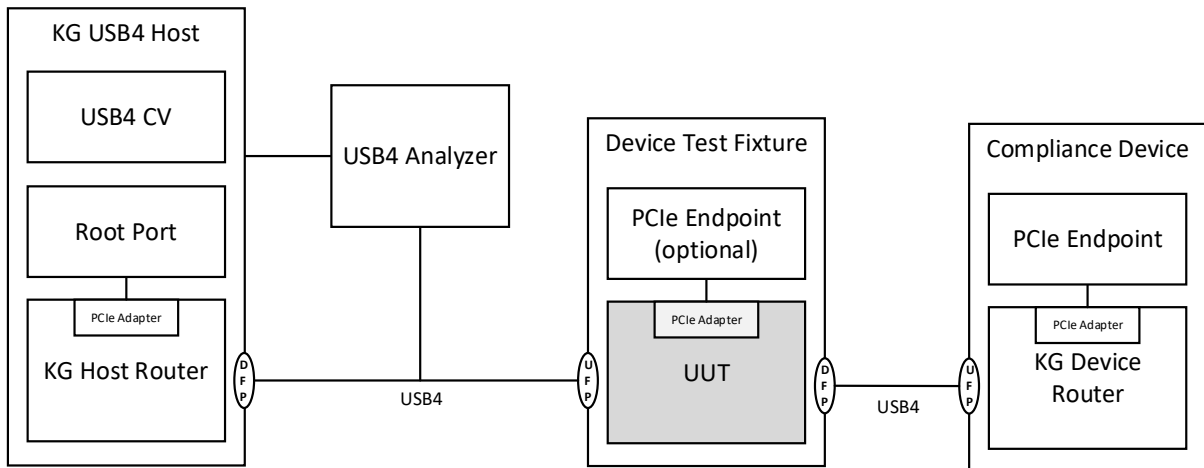


Hub

This section describes the test setups for a Hub Router (i.e. a Device Router with one or more DFP).

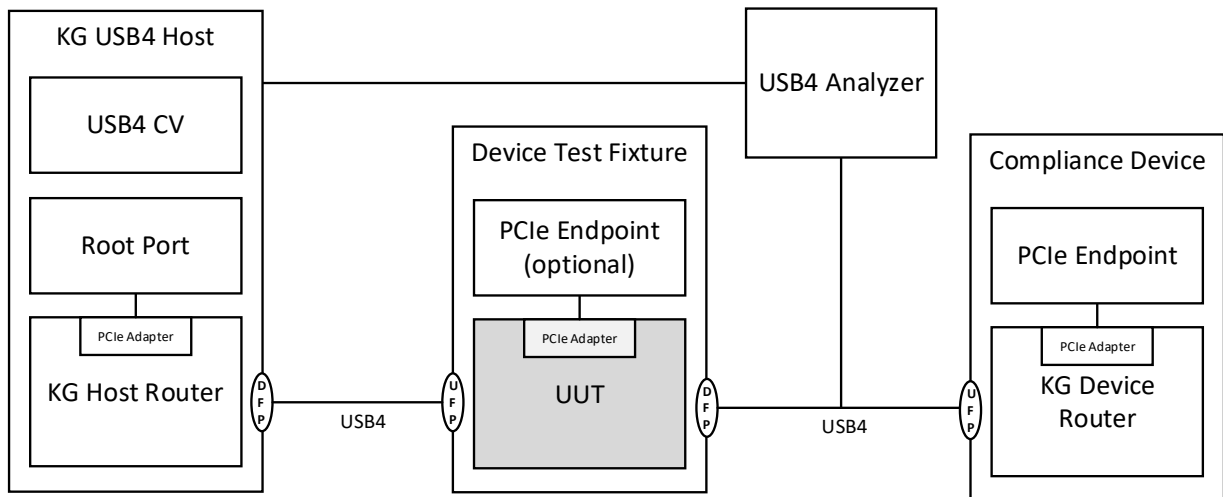
AN_HUB_UFP1+AN_HUB_UFP2—PCIE_01

- If the UUT includes an embedded PCIe endpoint, the vendor provides a Windows driver/utility capable of running controlled Tx/Rx traffic on the device.
- A KG USB4 Host is connected to the UUT.
 - Host supports PCIe tunneling
 - Host supports ASPM L1 on all USB4 Ports
- A USB4 Analyzer is connected between the KG USB4 Host and UUT.
- A USB4 Analyzer is connected between the KG USB4 Host and UUT.
- A Compliance Device with a known PCIe endpoint is connected to the DFP of the UUT.
 - The PCIe endpoint has the means to generate a PCIe wake under SW control



AN_HUB_DFP1—PCIE_02

- If the UUT includes an embedded PCIe endpoint, the vendor provides a Windows driver/utility capable of running controlled Tx/Rx traffic on the device.
- A known host system running Windows OS with a KG USB4 Host will connect to the UUT.
 - Host supports PCIe tunneling
 - Host supports ASPM L1 on all USB4 Ports
- A Compliance Device with a known PCIe endpoint is connected to the DFP of the UUT.
 - The PCIe endpoint has the means to generate a PCIe wake under SW control

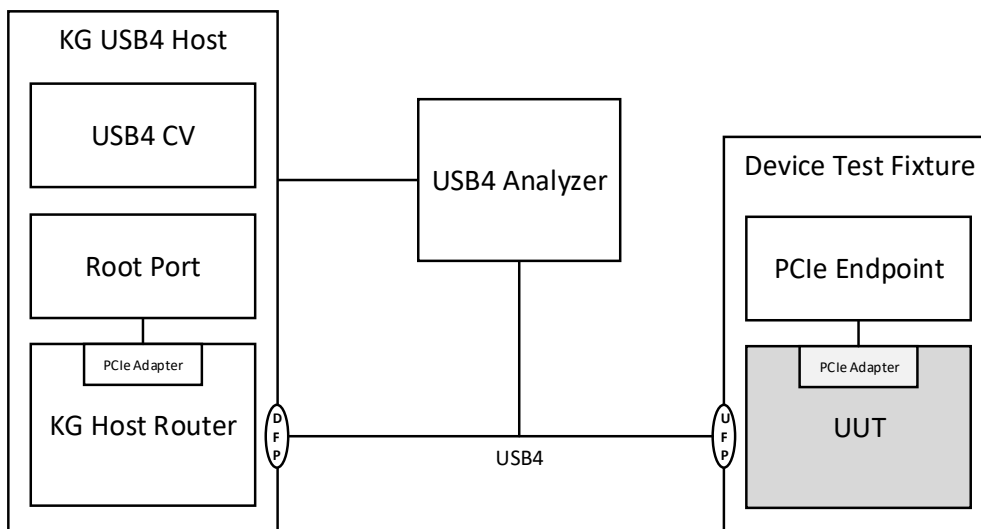


Peripheral Device

This section describes the test setup for a Peripheral Device Router (i.e. a Device Router that does not have DFP).

AN_DEV_UFP1—PCIE_01

- Vendor provides device test fixture for the UUT with a x8 PCIe slot.
- For an embedded PCIe endpoint, the vendor provides a Windows driver/utility capable of running controlled Tx/Rx traffic on the device.
- A KG USB4 Host is connected to the UUT.
 - Host supports PCIe tunneling
 - Host supports ASPM L1 on all USB4 Ports
- A USB4 Analyzer is connected between the KG USB4 Host and UUT.



Test Requirements

Test SW and HW

- Compliance Host System:
- OS and compliance HW support MPS of at least 256B
- Host system may report a wake event from the Host Router (TD11.101)

Compliance Device System:

- Compliance Device can issue read requests $\geq 256B$
- PCIe devices can be put into D3 (hot or cold) state
- Compliance Device supports PCIe wake and provides the means to generate a PCIe wake by USB4 CV

UUT

Hosts:

- UUT provides the means for traffic generation control as defined below
- A Host Router UUT provides the means to verify execution of write requests by the UUT

Hubs/Devices:

- UUT provides the means for traffic generation control as defined below
- A Device Router UUT provides the means to verify execution of read request completions by the UUT
- A Device Router UUT that supports PCIe wake provides the means to generate a PCIe wake by USB4 CV
– Open: how?

Traffic Generation Control

Note: This section only applies to USB4 hubs and devices that contain an embedded PCIe endpoint.

In order to test the USB4 PCIe Tunnel with PCIe traffic, a Vendor shall do one of the following:

- Supply a Batch file (.bat) as described below, which can control the PCIe traffic generation from the Vendor DUT.
- Specify an existing application (e.g., a benchmark tool) to stimulate PCIe traffic generation from the Vendor DUT.

Open: when executing a read request from a device UUT, the utility needs to report that the read completion was executed correctly. How is it done?

Batch File name:

Vendor's choice. On relevant tests, pop-up windows will be used to choose the file location.

Batch File Description:

DUT generates a sequence of read or write requests to host memory. Each request reads or writes <size> number of bytes from / to host memory. Requests are sent every <interval> time. A single sequence runs at any given time.

Batch File Parameters:

1. -start : To start traffic generation.
2. -type (read=0b, write=1b): type of traffic generated by the DUT.
3. -size: Number of bytes read / written from/to host memory in a single request.
4. -dump : Dump file location, Created by USB4CV software. Used by the batch file to write errors.
5. -interval : Time[ms] interval between each packet.
6. -stop : To stop traffic generation.

Batch File Format:

1. To start read traffic of 1 KB with 1 ms intervals:
`gen.bat -start -type 0 -size 1024 -interval 1 -dump "C:\\Users\\Public\\USB4\\Traffic\\trafficDump.txt"`
2. To start write traffic of 1 KB with 1 ms intervals:
`gen.bat -start -type 1 -size 1024 -interval 1 -dump "C:\\Users\\Public\\USB4\\Traffic\\trafficDump.txt"`
3. To stop traffic:
`gen.bat -stop`

Batch File Status:

If the dump file remains empty, the traffic generation is assumed to be without errors. If the dump file is not empty, the traffic generation is assumed to have errors, which are described in the dump file.

Test Descriptions

Unless specified otherwise, the tests in this section are performed in USB4 mode where all connected USB4 Ports negotiate and enter USB4 operation as described in the USB Type-C Specification and the USB PD Specification. USB4 CV enumerates the Router as a USB4 Connection Manager.

Tests are performed at the highest signaling speed that the UUT supports. Lanes are bonded unless specified otherwise. When Lanes are bonded, the configuration Space of the Lane 0 Adapter is used to perform the tests.

Unless otherwise noted, a test will timeout if it takes more than 500ms to go from one step to the next step. It is a test failure if a test times out.

Background Check Procedure

The test steps in this section are performed by the Analyzer in the background while the rest of the tests in this document are performed.

1. Parse each USB4 Transaction – Check for correct USB4 header and identify PCIe Tunneled Packets
2. Parse each PCIe Transaction:
 - a. For TLP Check Type, LEN, CHK fields and END symbol
 - b. For DLLP check SDP and END symbol
 - c. For OS check TS fields – Link Number, Lane Number, N_FTS, Data rate identifier, Training control
 - d. For EIOS, check for correct symbols
 - e. Identify PERST#
3. For TLP's DLLP's – check correctness at the PCIe level as defined by the PCIe 4.0 specification

PCIe Tunneling Tests

TD 11.001 Product Structure Test

Note: This test is only performed once on the UUT.

A. Purpose:

- Verify that the UUT includes a PCIe switch or endpoint

B. Asserts:

- 11#1, 11#3, 11#5

C. Test Setup:

- AN_HOST_DFP1—PCIE_01 (Host)
- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Procedure:

Case 1 – USB4 Host

1. Power on the UUT
2. Enumerate the UUT on the host system
3. Verify that the UUT contains either a PCIe switch or a root port

Case 2 – USB4 Peripheral Device

1. Connect the UUT to the host system
2. Enumerate the UUT on the PCIe bus through the Host Router
3. Verify that the UUT contains a PCIe switch and/or a PCIe endpoint

Case 3 – USB4 Hub

1. Connect the UUT to the host system
2. Enumerate the UUT on the PCIe bus through the Host Router
3. Verify that the UUT contains a PCIe switch

TD 11.002 Supported Tunnel Speed Test

Note: This test is only performed once on the UUT.

A. Purpose:

- Verify that the UUT only supports GEN1 speed when tunneling PCIe

B. Asserts:

- 11.2.1#1

C. Test Setup:

- AN_HOST_DFP1—PCIE_01 (Host)
- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Procedure:

1. Connect the UUT
2. Enumerate the UUT
3. For each PCIe Port on the UUT:
 - a. Read the Link Capabilities register from PCIe configuration space
 - b. Verify that the max link speed field is GEN1

TD 11.003 Unsupported LTSSM States Test

Note: This test is only performed once on the UUT.

A. Purpose:

- Verify that the UUT does not support non-required LTSSM states when tunneling PCIe

B. Asserts:

- 11.2.1.2#2

C. Test Setup

- AN_HOST_DFP1—PCIE_01 (Host)
- [AN_HUB_UFP2](#)—PCIE_01 (Hub)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Procedure:

1. Connect the UUT
2. Enumerate the UUT
3. For each PCIe Port on the UUT:
 - a. Read the ASPM support bits from the Link Capabilities register
 - b. Verify that L0s is not supported
 - c. Verify that L1 PM sub-states capability does not exist on the PCIe port

A. Purpose:

- Verify that the UUT handles Hot Reset (secondary bus reset) correctly over a PCIe tunnel

B. Asserts:

- 11.2#1

C. Test Setup:

- AN_HOST_DFP1—PCIE_01 (Host)
- AN_HUB_DFP1—PCIE_02 (Hub DFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Repetitions:

Repeat for each Downstream PCIe Adapter in the UUT

E. Procedure:

Part 0 – Setup

1. Start the Analyzer
2. Reset the UUT
3. Configure the UUT and Compliance Device (if connected)
4. Set PCIe Paths to the UUT and Compliance Device (if connected)
5. Enumerate and configure the PCI functions in the UUT and Compliance Device (if connected)

Part 1 – Upstream Behavior

6. Disable hot plug interrupts on the PCIe Downstream port above the UUT

Note: Hot plug interrupts are disabled by zeroing the Presence Detect Changed Enable, Hot-Plug Interrupt Enable and Data Link Layer State Changed Enable bits on the slot control register.

7. From the PCIe Downstream port above the UUT, perform a secondary bus reset from the bridge control register

Note: A secondary bus reset propagates an in-band reset to the UUT. This is called a “hot reset”.

8. Read DW0 in the PCI Common Configuration Space of the PCIe upstream port in the UUT
9. Verify that the UUT does not respond to the Read Request to DW0 (11.2#1)
10. Exit hot reset
11. Verify that the UUT PCIe Upstream port is responding to accesses (11.2#1)
12. Verify that the configuration space was reset by checking the Command (CMD offset 0x4) MMIO and BME bits and the Bus register (offset 0x18) primary, secondary, and subordinate fields (11.2#1)

Part 2 – Downstream Behavior (Hosts and Hubs only)

13. Reconfigure the PCIe port bus range through the PCIe access SW
14. Verify the hot reset propagation (i.e. the ports below were also reset) (11.2#1)
15. For every Downstream PCIe Adapter in the UUT:
 - a. Reset the Compliance Device
 - b. Enumerate the Compliance Device
 - c. Establish a PCIe tunnel to the Compliance Device
 - d. Configure the Compliance Device according to the PCIe specification
 - e. Disable hot plug interrupts as specified above
16. Perform hot reset from the bridge control register of the PCIe port connected to the Downstream PCIe Adapter
17. Verify that the upstream port in the Compliance Device was reset (11.2#1)
18. Parse the Analyzer trace and verify the following:
 - a. The TS1/TS2 structure is correct
 - b. The Hot Reset bit (bit[0] in symbol 5 (Training Control) is set to 1b in two consecutive TS1 Ordered Sets
19. Stop the Analyzer

TD 11.005 Link Bring Up and Retrain Test

A. Purpose:

- Verify that the UUT brings up correctly the PCIe link over a tunnel
- Verify that the UUT handles PCIe link retrain correctly over a tunnel

B. Asserts:

- 11.2#1, 11.1.1.2.1#1, 11.1.1.2.1#2, 11.1.1.2.1#3, 11.1.1.2.1#4, 11.1.1.2.2#1, 11.1.1.2.2#2

C. Test Setup:

- AN_HOST_DFP1—PCIE_01 (Host)
- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)
- AN_HUB_DFP1—PCIE_02 (Hub DFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Repetitions:

Repeat for the UFP and each DFP of the UUT

E. Procedure:

Part 0 - Setup

1. Reset UUT
2. Configure the UUT and Compliance Device

Part 1 - Link Bring Up

3. Start the Analyzer
4. Set PCIe Paths to the UUT and Compliance Device
5. Enumerate and configure PCI functions in the UUT and Compliance Device
6. Stop the Analyzer

Part 2 – Verification:

7. Read the LTSSM field from the PCIe Adapter
8. Verify that the LTSSM is in L0 [or L1](#) (11.2#1)
9. Verify that each TS1 flavor (Different payload) is presented consecutively at least 16 times (11.1.1.2.1#1)
 - a. Verify there is at least one flavor of TS1
10. Verify that each TS2 flavor (Different payload) is presented consecutively at least 16 times (11.1.1.2.1#2)
 - a. Verify there is at least one flavor of TS2
11. For each TS1 and TS2 Tunneled Packet verify in payload (11.1.1.2.1#4)
 - a. Byte 0 in payload equals 0xBC
 - b. Byte 2 (Lane Number) equals 0 or 0xF7 (11.1.1.2.1#3)
 - c. Byte 4 (Data Rate Identifier) equals to 0x02 (2.5 GT/s)

- d. Bytes 6-15 equals to 0x4A for TS1 and 0x45 for TS2
- 12. Verify that the PCIe port at the Compliance Device is accessible on the PCIe bus (11.2#1)

Part 3 – Link Re-train

- 13. Start the Analyzer
- 14. Perform link retrain by setting the *Retrain Link* bit in the *Link Control register* of the port:
 - a. UFP: From the PCIe Downstream port above the UUT
 - b. DFP: From the PCIe port associated with the PUT
- 15. Wait 1 second
- 16. Stop Analyzer
- 17. Repeat the Verification steps (Steps 7 through 12)

A. Purpose:

- Verify that the UUT handles link disable correctly over a PCIe tunnel

B. Asserts:

- 11.2#1, 11.1.1.2.1#1, 11.1.1.2.1#2, 11.1.1.2.1#3, 11.1.1.2.1#4

C. Test Setup:

- AN_HOST_DFP1—PCIE_01 (Host)
- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)
- AN_HUB_DFP1—PCIE_02 (Hub DFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Repetitions:

- Repeat for the UFP and each DFP of the UUT

E. Procedure:

Part 0 - Setup

1. Start the Analyzer
2. Reset UUT
3. Configure the UUT and Compliance Device
4. Set PCIe Paths to the UUT and Compliance Device
5. Enumerate and configure PCI functions in the UUT and Compliance Device
6. If the PUT is a UFP, perform Part 1 or if the UUT is a DFP, perform Part 2

Part 1 – UFP Test

7. Disable hot plug interrupts on the PCIe Downstream port above the UUT

Note: Hot plug interrupts are disabled by zeroing the Presence Detect Changed Enable, Hot-Plug Interrupt Enable and Data Link Layer State Changed Enable bits on the slot control register

8. Perform link disable from the PCIe Downstream port above the UUT

Note: This is done by setting the Link Disable bit in the link control register

9. Verify that the link went to disabled state and the UUT is not responding to access (11.2#1)
10. Set the *Link Disable* bit to 0
11. Verify that the PCIe link trains back up to L0 [or L1](#) (11.2#1)
12. Verify that at least 16 replicas of TS1 and TS2 are generated by the PUT (11.1.1.2.1#1, 11.1.1.2.1#2)
13. Verify that the UUT is accessible on the PCIe bus (11.2#1)

Part 1 – DFP Test

14. Connect the Compliance Device to the PUT
15. Enumerate the Compliance Device
16. Disable hot plug interrupts in the PCIe port associated with the PUT as specified above
17. Perform link disable from the PCIe port's link control register
18. Verify that the link went to disabled state by reading the LTSSM (11.2#1)
19. Verify that the link goes down and trains back up to L0 [or L1](#) (11.2#1)
20. Verify that at least 16 replicas of TS1 and TS2 are generated by the PUT (11.1.1.2.1#1, 11.1.1.2.1#2)
21. Verify that the PCIe upstream port in the Compliance Device is accessible (11.2#1)
22. Stop the Analyzer

A. Purpose:

- Verify that the UUT PCIe link is correctly entering and exiting ASPM L1 on a supporting tunnel

B. Asserts:

- 11.2#1, 11.2.1.2#1, 11.1.1.2.2#1, 11.1.1.2.2#2, 11.1.1.3#1, 11.1.1.3#2

C. Test Setup

- AN_HOST_DFP1—PCIE_01 (Host)
- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)
- AN_HUB_DFP1—PCIE_02 (Hub DFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Repetitions

Repeat for each USB4 Port

E. Procedure:

Part 0 - Setup

1. Start the Analyzer
2. Reset UUT
3. Configure the UUT and Compliance Device
4. Set PCIe Paths to the UUT and Compliance Device
5. Enumerate and configure PCI functions in the UUT and Compliance Device
6. If the PUT is a DFP, perform Part 1
7. If the UUT is a Hub UFP, perform Part 2
8. If the UUT is a Peripheral Device UFP, perform Part 3

Part 1 – DFP Test

9. Read the PCIe Link Capabilities register of the PCIe port associated with the PUT
10. If ASPM L1 is not supported, end test here
11. Enable ASPM L1 in the PCIe Link Control register of the PCIe port

Note: From the PCIe spec: “When supported, L1 entry is disabled by default in the ASPM Control field. Software must enable ASPM L1 on the Downstream component only if it is supported by both components on a Link. Software must sequence the enabling and disabling of ASPM L1 such that the Upstream component is enabled before the Downstream component and disabled after the Downstream component.”

12. Enable ASPM L1 in the Link Partner
13. Wait for 1 second
14. Read the LTSSM field in the PCIe Adapter Configuration Capability of the PUT
15. Verify that the current state is L1 (11.2.1.2#1)

16. Parse the Analyzer trace and verify that:
 - a. The L1 entry handshake is as defined by the PCIe specification (11.2.1.2#1)
 - b. Transmission of 2 consecutive EIOS by the UUT (11.1.1.2.2#1)
 - c. Transmission of at least three consecutive Electrical Idle State Tunneled Packet by the UUT (11.1.1.3#1)
17. Configure the Compliance Device to generate write traffic to host memory for 100 ms, alternating between an active 1 ms period and an idle 1 ms period.
18. Read the LTSSM field in the PCIe Adapter Configuration Capability of the PUT periodically
19. Verify alternating between entry to L1 state and exit from L1 state (11.2.1.2#1)
20. Generate write requests to the Compliance Device every 1 ms for a period of 100 ms,
21. Read the LTSSM field in the PCIe Adapter Configuration Capability of the PUT periodically
22. Verify alternating between entry to L1 state and exit from L1 state (11.2.1.2#1)

Part 2 – Hub UFP Test:

Note: Perform with the Compliance Device connected to a Port that supports ASPM L1, if exists

23. Read the PCIe Link Capabilities register of the PCIe port associated with the PUT
24. If ASPM L1 is not supported, end test here
25. Enable ASPM L1 in the host port connected to the PUT
26. Enable ASPM L1 in the PCIe Link Control register of the PCIe port associated with the PUT
27. If ASPM is supported by the DFP connected to the Compliance Device
 - a. Enable ASPM L1 in the PCIe Link Control register of the DFP
 - b. Enable ASPM L1 in the Link partner
28. Wait for 1 second
29. Read the LTSSM field in the PCIe Adapter Configuration Capability of the host PCIe port
30. Verify that the current state is L1 (11.2.1.2#1)
31. Parse the Analyzer trace and verify that:
 - a. The L1 entry handshake is as defined by the PCIe specification (11.2.1.2#1)
 - b. The UUT transmitted 2 consecutive EIOS (11.1.1.2.2#1)
 - c. The UUT transmitted at least three consecutive Electrical Idle State Tunneled Packets (11.1.1.3#1)
32. Configure the Compliance Device to generate write traffic to host memory for 100 ms, alternating between an active 1 ms period and an idle 1 ms period.
33. Read the LTSSM field in the PCIe Adapter Configuration Capability of the host PCIe port periodically
34. Verify alternating between entry to L1 state and exit from L1 state (11.2.1.2#1)
35. Generate write requests to the Compliance Device every 1 ms for a period of 100 ms,
36. Read the LTSSM field in the PCIe Adapter Configuration Capability of the host PCIe port periodically
37. Verify alternating between entry to L1 state and exit from L1 state (11.2.1.2#1)

Part 3 – Peripheral UFP Test:

38. Read the PCIe Link Capabilities register of the PCIe port associated with the PUT
39. If ASPM L1 is not supported, end test here
40. Enable ASPM L1 in the host port connected to the PUT
41. Enable ASPM L1 in the PCIe Link Control register of the PCIe port associated with the PUT
42. Wait for 1 second

43. Read the LTSSM field in the PCIe Adapter Configuration Capability of the host PCIe port
44. Verify that the current state is L1 (11.2.1.2#1)
45. Parse the Analyzer trace and verify that:
 - a. The L1 entry handshake is as defined by the PCIe specification (11.2.1.2#1)
 - b. The UUT transmitted 2 consecutive EIOS (11.1.1.2.2#1)
 - c. The UUT transmitted at least three consecutive Electrical Idle State Tunneled Packets (11.1.1.3#1)
46. Configure the Compliance Device to generate write traffic to host memory for 100 ms, alternating between an active 1 ms period and an idle 1 ms period.
47. Read the LTSSM field in the PCIe Adapter Configuration Capability of the host PCIe port periodically
48. Verify alternating between entry to L1 state and exit from L1 state (11.2.1.2#1)
49. Generate write requests to the Compliance Device every 1 ms for a period of 100 ms,
50. Read the LTSSM field in the PCIe Adapter Configuration Capability of the host PCIe port periodically
51. Verify alternating between entry to L1 state and exit from L1 state (11.2.1.2#1)

TD 11.008 PM L1 Nak Response Test (Hubs and Devices Only)

A. Purpose:

- Verify correct behavior of the PCIe upstream port when sending PM_Active_State_Nak DLLP

B. Asserts:

- 11.2.1.3#1

C. Test Setup

- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Repetitions:

Repeat for each USB4 Port that supports PCIe Tunneling

E. Procedure:

Part 0 - Setup

1. Start the Analyzer
2. Reset UUT
3. Configure the UUT and Compliance Device
4. Set PCIe Paths to the UUT and Compliance Device
5. Enumerate and configure PCI functions in the UUT and Compliance Device

Part 1 – UFP Test

6. Read the PCIe Link Capabilities register of the PCIe port associated with the PUT
7. If ASPM L1 is not supported, end test here
8. Enable L1 on the UUT PCIe upstream port (but not on the opposite downstream port)
9. Capture (using the USB4 analyzer) the PCIe flow that starts with a PM_Active_State_Request_L1 DLLP
10. Verify that PM_Active_State_Request_L1 DLLPs are generated by the upstream port and answered by PM_Active_State_Nak DLLP (11.2.1.2#1)
11. Verify that no more than 10 PM_Active_State_Request_L1 DLLPs are sent by the upstream port after sending an ACK DLLP for the received PM_Active_State_Nak message (11.2.1.3#1)
12. Enable L1 on the downstream port connected to the UUT
13. Wait for 1 second
14. Read the LTSSM field in the PCIe Adapter Configuration Capability of the host PCIe port
15. Verify that the current LTSSM state is L1 (11.2.1.2#1)

TD 11.009 SW Controlled L1 and L2 Test

A. Purpose:

- Verify that the UUT enters and exits L1 and L2 properly under SW control

B. Asserts:

- 11.2#1

C. Test Setup:

- AN_HOST_DFP1—PCIE_01 (Host)
- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)
- AN_HUB_DFP1—PCIE_02 (Hub DFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Repetitions:

- Repeat for the UFP and each DFP of the UUT

E. Procedure:

Part 0 - Setup

1. Start the Analyzer
2. Reset UUT
3. Configure the UUT and Compliance Device
4. Set PCIe Paths to the UUT and Compliance Device
5. Enumerate and configure PCI functions in the UUT and Compliance Device

Part 1 – UFP Test

6. Initiate L1 entry at the PCIe upstream Port of the UUT by setting the PowerState field in the PCI Power Management Capability of the port to 11b (D3hot)

Note: In a multi-function endpoint, all functions need to be in D3 state. In a hub, the DFPs of the switch and the endpoint need to first enter D3 state.

7. Capture the DLLP exchange to enter L1 state
8. Verify the DLLP exchange to enter L1 state occurred as described in the PCIe spec (11.2.1.2#1)
9. Read the LTSSM field in the PCIe Adapter Configuration Capability of the host PCI downstream port connected to the PUT
10. Verify that the current LTSSM state is L1 (11.2.1.2#1)
11. Exit L1 state by setting the PowerState field in the PCI Power Management Capability of the port to 00b (D0)
12. Read the LTSSM field in the PCIe Adapter Configuration Capability of the host PCI downstream port connected to the PUT
13. Verify that the current LTSSM state is L0 (11.2#1)
14. Initiate L1 entry at the PCIe upstream Port of the UUT:
15. Verify that the current LTSSM state is L1 (11.2.1.2#1)
16. Initiate L2 entry by triggering broadcast of PME_Turn_Off messages in the Domain

17. Capture the PME_Turn_Off / PME_TO_Ack exchange, followed by L2/L3 Ready transition protocol.
18. Verify the exchange to enter L2 state is as described in the PCIe spec (11.2#1)
19. Read the *LTSSM* field in the PCIe Adapter Configuration Capability of the host PCI downstream port connected to the PUT
20. Verify that the current state is L2 (11.2#1)
21. Exit L2 by assertion of PERST# to the UUT, followed by de-assertion of PERST#
22. Read the *LTSSM* field in the PCIe Adapter Configuration Capability of the host PCI downstream port connected to the PUT
23. Verify that the PCIe link reaches L0 (11.2#1)
24. Read DW0 in the PCI Common Configuration Space of the PCIe upstream port in the UUT
25. Verify the values of the *Vendor ID* field and the *Device ID* field (11.2#1)

Part 2 – DFP Test

26. Initiate L1 entry at the PCIe upstream Port of the Compliance Device by setting the PowerState field in the PCI Power Management Capability of the port to 11b (D3hot)
27. Capture the DLLP exchange to enter L1 state
28. Verify the DLLP exchange to enter L1 state occurred as described in the PCIe spec (11.2.1.2#1)
29. Read the *LTSSM* field in the PCIe Adapter Configuration Capability of the PCI downstream port connected to the PUT
30. Verify that the current state is L1 (11.2.1.2#1)
31. Exit L1 state by setting the PowerState field in the PCIe upstream Port of the Compliance Device to 00b (D0)
32. Read the *LTSSM* field in the PCIe Adapter Configuration Capability of the PCI downstream port connected to the PUT
33. Verify that the current state is L0 (11.2#1)
34. Initiate L1 entry at the PCIe upstream Port of the Compliance Device:
35. Read the *LTSSM* field in the PCIe Adapter Configuration Capability of the PCI downstream port connected to the PUT
36. Verify that the current state is L1 (11.2.1.2#1)
37. Initiate L2 entry by triggering broadcast of PME_Turn_Off messages in the Domain
38. Capture the PME_Turn_Off / PME_TO_Ack exchange, followed by L2/L3 Ready transition protocol.
39. Verify the exchange to enter L2 state is as described in the PCIe spec (11.2#1)
40. Read the *LTSSM* field in the PCIe Adapter Configuration Capability of the PCI downstream port connected to the PUT
41. Verify that the current state is L2 (11.2#1)
42. Exit L2 by assertion of PERST# to the UUT, followed by de-assertion of PERST#
43. Read the *LTSSM* field in the PCIe Adapter Configuration Capability of the PCI downstream port connected to the PUT
44. Verify that the PCIe link reaches L0 (11.2#1)
45. Read DW0 in the PCI Common Configuration Space of the PCIe upstream port in the Compliance Device
46. Verify the values of the *Vendor ID* field and the *Device ID* field (11.2#1)

TD 11.010 Max Payload Size Support Test (Ver. 1 Only)

A. Purpose:

- Verify that the UUT ports support only 128B max payload size

B. Asserts:

- 11.2.3#1

C. Test Setup:

- AN_HOST_DFP1—PCIE_01 (Host)
- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)
- AN_HUB_DFP1—PCIE_02 (Hub DFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Procedure:

1. Connect UUT
2. Enumerate the UUT
3. For each embedded PCIe device in the UUT:
 - a. Read the device capabilities register
 - b. Verify that the Max_Payload_Size supported field declares 128B support

Note: To maximize latency on the USB4 Link, the Test Setups for this test use an active cable with 2 Re-timers and a KG host with 2 Re-timers.

A. Purpose:

- Verify that the UUT can pass high BW PCIe traffic without recoveries and errors

B. Asserts:

- 11.2#1

C. Test Setup

- AN_HOST_DFP1—PCIE_01 (Host)
- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)
- AN_HUB_DFP1—PCIE_02 (Hub DFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Repetitions:

- Repeat for each DFP of a Host UUT
- Repeat for the UFP and each DFP of a Hub UUT

E. Procedure:

Part 0 – Setup

1. Start the Analyzer
2. Reset UUT
3. Configure the UUT and Compliance Device
4. Set PCIe Paths to the UUT and Compliance Device
5. Enumerate and configure PCI functions in the UUT and Compliance Device

Part 1 – Test

6. Initiate PCIe Tx/Rx traffic over the PUT for the equivalent of 10 to 100 seconds
7. Verify with the USB4 analyzer that the number of bytes transmitted or received by the PUT equals the amount scheduled to within 10%. (11.2#1)
8. Verify with the USB4 analyzer that no PCIe TS1 are exchanged through the PUT (i.e., no PCIe link recoveries on the tunnel) (11.2#1)
9. Verify that no uncorrectable PCIe errors were reported in the Uncorrectable Error Status Register of the Advanced Error Reporting Extended Capability (i.e. all bits are set to 0b) in the Link Partner (11.2#1)
10. If Advanced Error Reporting is supported by the UUT, verify that no uncorrectable PCIe errors were reported in the Uncorrectable Error Status Register of the Advanced Error Reporting Extended Capability (i.e. all bits are set to 0b) in the UUT (11.2#1)

11. Verify that no correctable PCIe errors were reported in the Correctable Error Status Register of the Advanced Error Reporting Extended Capability in the Link Partner as follows (11.2#1):
 - a. Bad TLP Status bit = 0b
 - b. Bad DLLP Status bit = 0b
 - c. REPLAY_NUM Rollover Status bit = 0b
12. If Advanced Error Reporting is supported by the UUT, verify that no correctable PCIe errors were reported in the Correctable Error Status Register of the Advanced Error Reporting Extended Capability in the UUT as follows (11.2#1):
 - a. Bad TLP Status bit = 0b
 - b. Bad DLLP Status bit = 0b
 - c. REPLAY_NUM Rollover Status bit = 0b

A. Purpose:

- Verify PTM functionality. Mandatory for a USB4 hub. Optional otherwise

B. Asserts:

- 11.2.5#1, 11.2.5.1#1, 11.2.5.2#2, 11.2.5.2#4

C. Test Setup:

- AN_HOST_DFP1—PCIE_01 (Host)
- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)
- AN_HUB_DFP1—PCIE_02 (Hub DFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Repetitions:

- Repeat for the UFP and each DFP of the UUT

E. Procedure:

Part 0 - Setup

1. Start the Analyzer
2. Reset UUT
3. Configure the UUT and Compliance Device
4. Set PCIe Paths to the UUT and Compliance Device
5. Enumerate and configure PCI functions in the UUT and Compliance Device

Part 1 –Test

6. If the UUT is a host:
 - a. Read the PTM capability structure in the PCIe upstream port associated of the switch connected to the UUT.
 - b. If a PTM capability structure does not exist, end test here.
 - c. Verify that it complies with the PCIe 4.0 specification
7. If the UUT is a hub:
 - a. Read the PTM capability structure in the PCIe port associated with the UFP
 - b. If a PTM capability structure does not exist, end test here
 - c. Verify that it complies with the PCIe 4.0 specification
8. If the UUT is a device:
 - a. Read the PTM capability structure in the PCIe port associated with the UFP
 - b. If a PTM capability structure does not exist, end test here.
 - c. Verify that it complies with the PCIe 4.0 specification
9. Enable PTM by setting the PTM enable bit to 1b, starting from the host and moving towards the leaves of the PCIe sub-hierarchy
10. Parse the Analyzer trace and verify that the PTM Msg and MsgD packet exchange occurs as described in the PCIe 4.0 specification

TD 11.013 Deprecated

TD 11.014	Deprecated
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TD 11.015	Deprecated
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TD 11.016 LTR Support Test (Hubs and Devices Only)

A. Purpose:

- Verify that the UUT supports the LTR capability

B. Asserts:

- 11.2.3#2

C. Test Setup:

- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Procedure:

Part 0 - Setup

1. Start the Analyzer
2. Reset UUT
3. Configure the UUT and Compliance Device
4. Set PCIe Paths to the UUT and Compliance Device
5. Enumerate and configure PCI functions in the UUT and Compliance Device

Part 1 – Test

6. Read the LTR capability structure in the PCIe upstream port of the UUT
7. Verify that it complies with the PCIe 4.0 specification (11.2.3#2)

TD 11.017 Hot-Plug Support Test (Hosts and Hubs Only)

A. Purpose:

- Verify that the UUT supports hot-plug

B. Asserts:

- 11.2.3#3, 11.1.2#2

C. Test Setup:

- AN_HOST_DFP1—PCIE_01 (Host)
- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)

D. Procedure:

Part 0 - Setup

1. Start the Analyzer
2. Reset UUT
3. Configure the UUT and Compliance Device
4. Set PCIe Paths to the UUT and Compliance Device
5. Enumerate and configure PCI functions in the UUT and Compliance Device

Part 1 - Test

6. Do not configure a PCIe tunnel on any of the UUT's DFPs
7. Read the Slot Capabilities Register of each PCIe downstream port in the UUT that is connected to a Downstream PCIe Adapter
8. Verify that the *Hot-Plug Surprise* bit and *Hot-Plug Capable* bit are set to 1b (11.2.3#3)
9. Set to 1b the *Presence Detect Changed Enable* bit and the *Hot-Plug Interrupt Enable* bit in the Slot Control Register.
10. Read the Slot Control Register
11. Verify that the *Presence Detect Changed Enable* bit and the *Hot-Plug Interrupt Enable* bit are set to 1b (11.2.3#3)

TD 11.018 ACS Support Test (Hubs Only)

A. Purpose:

- Verify that the UUT supports the ACS capability

B. Asserts:

- 11.2.3#4

C. Test Setup:

- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)

D. Procedure:

Part 0 - Setup

1. Start the Analyzer
2. Reset UUT
3. Configure the UUT and Compliance Device
4. Set PCIe Paths to the UUT and Compliance Device
5. Enumerate and configure PCI functions in the UUT and Compliance Device

Part 1 - Test

6. Read the ACS capability structure from each PCIe downstream port in the UUT
7. Verify that it complies with the PCIe 4.0 specification (11.2.3#4)

TD 11.019 FPB Support (Hub Only) Test

A. Purpose:

- Verify that the UUT supports the FPB capability

B. Asserts:

- 11.2.3#5

C. Test Setup:

- [AN_HUB_UFP2](#)—PCIe_01 (Hub UFP)

D. Procedure:

Part 0 - Setup

1. Start the Analyzer
2. Reset UUT
3. Configure the UUT and Compliance Device
4. Set PCIe Paths to the UUT and Compliance Device
5. Enumerate and configure PCI functions in the UUT and Compliance Device

Part 1 - Test

6. Read the FPB Capability Structure from each PCIe port connected to a PCIe Adapter in the UUT
7. Verify that each FPB Capability Structure complies with the PCIe 4.0 specification (11.2.3#5)

TD 11.020 Path Teardown Test

A. Purpose:

- Verify that the UUT tears down the PCIe Path upon a disconnect event

B. Asserts:

- 11.3.2#1, 11.3.2#2, 11.1.2#1, 11.1.2#2

C. Test Setup:

- AN_HOST_DFP1—PCIE_01 (Host)
- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)
- AN_HUB_DFP1—PCIE_02 (Hub DFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Repetitions:

Repeat for the UFP and each DFP of the UUT

E. Procedure:

Part 0 - Setup

1. Start the Analyzer
2. Reset UUT
3. Configure the UUT and Compliance Device
4. Set PCIe Paths to the UUT and Compliance Device
5. Enumerate and configure PCI functions in the UUT and Compliance Device
6. Disable ASPM by writing 0 to the ASPM Control bits in the Link Control register in the PCIe Capability Structure for each PCIe port.
7. If the PUT is a UFP, perform Part 1; if the PUT is a DFP, perform Part 2

Part 1 – UFP Test

8. Disconnect the UUT
9. Tear down the PCIe Paths at the Host Router
10. Wait 1 second
11. Reconnect the UUT
12. Enumerate the UUT, but do not set up any PCIe Paths
13. Read the *Path Enable* bit from the Upstream PCIe Adapter
14. Verify that the *Path Enable* bit is 0b (11.3.2#1)
15. Verify that the *RST* bit in the upstream PCIe adapter is 1b (11.1.2#1)
16. Set PCIe Paths with the UUT
17. Verify that the *RST* bit in the Upstream PCIe adapter is 0b (11.1.2#2)
18. Read the LTSSM field from the Upstream PCIe Adapter
19. Verify that the LTSSM field is 6h (L0 state) [or 7h \(L1 state\)](#) (11.2#1)

Part 2 – DFP Test

20. Disconnect the compliance device
21. Read the *Path Enable* bit from the Downstream PCIe Adapter corresponding to the PUT that the KG USB4 Device was connected to
22. Verify that the *Path Enable* bit is 0b (11.3.2#1)
23. Read the LTSSM field from the Downstream PCIe Adapter corresponding to the PUT that the KG USB4 Device was connected to
24. Verify that the LTSSM field is 00h (DETECT state) (11.3.2#3)
25. Tear down PCIe Paths at the Host Router
26. Reconnect the Compliance Device
27. Set PCIe Paths with the Compliance Device
28. Read the *LTSSM* field from the Downstream PCIe Adapter corresponding to the PUT that the KG USB4 Device was connected to
29. Verify that the LTSSM field is 6h (L0 state) [or 7h \(L1 state\)](#) (11.2#1)

TD 11.101 Nullified TLPs Test (Hubs Only)

A. Purpose:

- Verify that a USB4 hub handles nullified TLPs properly

B. Asserts:

- 11.1.1.1.3#100,106

C. Test Setup:

- EX_HUB_UFP1—PCIE_03 (Hub UFP)

D. Repetitions:

- Repeat for various sizes of nullified TLPs (<252B, >252B, >512B) within the system MPS

E. Procedure:

Part 0 - Setup

1. Set host to operate with MPS=256B
2. Reset the Domain by asserting Host Router Reset
3. Configure the host and any device below it
4. Set PCIe Paths from the host and in any device below it
5. Enumerate and configure PCI functions

Part 1 - Test

6. In the Compliance Hub, generate a nullified TLP directed to the host.
7. Verify (with the USB4 analyzer) that the nullified TLP is either dropped or passed to the host with the correct structure (11.1.1.1.3#10)

TD 11.102 PCIe Wake in Enumerated State (Hosts and Devices Only)

Note: This test applies to Host Routers that support systems with PCIe wake in enumerated state, and to Device Routers that generate PCIe Wake events. See contents of VIF.

A. Purpose:

- Verify a Device Router generates Notification Packet on PCIe wake
- Verify that a Host Router issues a wake to the host

B. Asserts:

- 11.1.4.2#100, 102, 103

C. Test Setup:

- AN_HOST_DFP1—PCIE_01 (Host)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Repetitions:

- Repeat for each DFP of a Host UUT

E. Procedure:

Part 0 - Setup

1. Reset the UUT
2. Enumerate the UUT and Routers below it
3. In the Device Router (Compliance Device or UUT) set the Enumerated State PCIe Wake bit in Router Configuration Space to 1b
4. Set PCIe Paths to the PCIe Endpoint
5. Configure each PCIe switch and endpoint along the PCIe Paths

Part 1 - Test

6. Set the Device Router (Compliance Device in Host test and UUT in other tests) into D3 state
7. Generate a PCI wake from the Device Router (Compliance Device in Host test and UUT in other tests)
8. Verify (w/ analyzer) that a Notification Packet with Event Code = PCIE_WAKE is sent over USB4 (Device Router test) (11.1.4.2#1)
9. Verify that a wake signal is sent to the host (Host Router test) (11.1.4.2#3)
10. Verify that a Notification Packet with Event Code = PCIE_WAKE reaches USB4 CV (11.1.4.2#4)

TD 11.103 ASPM L1 Test (Hubs and Devices Only)

Note: This test only applies when the USB4_TBT3_Compatibility_Supported bit in the VIF is set to YES for the UFP of the UUT.

A. Purpose:

- Verify that if TBT3 Mode is established on a Link and the USB4 Sideband Channel Support bit at the Link Partner is set to 0b, then ASPM L1 operation over PCIe Tunneling is disabled

B. Asserts:

- TBD

C. Test Setup:

- [AN_HUB_UFP2](#)—PCIE_01 (Hub UFP)
- AN_DEV_UFP1—PCIE_01 (Device)

D. Repetitions:

- None

E. Procedure:

Part 0 - Setup

1. Reset UUT
2. Configure the UUT and any device below it
3. Set PCIe Paths to the UUT and any device below it
4. Enumerate and configure PCI functions in the UUT and any device below it

Part 1 - Test

5. Read the TBT3-Compatible Mode bit in the USB4 Port Capability of the UUT's UFP.
6. Verify that the bit is set to 1b
7. Enable ASPM L1 in the host port connected to the UUT UFP
8. Enable ASPM L1 in the PCIe Link Control register of the PCIe port associated with the UFP
9. Wait for 1 second
10. Read the LTSSM field in the PCIe Adapter Configuration Capability of the host PCIe port
11. Verify that the current state is L0